Simulation of logic gates for Digital optical Networks using SOA

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Abstract: Optical gates are the basic elements required for performing all logic functions in digital optical processing. All optical logic gates are the basic performing unit in optical devices. through this paper, we propose all optical universal logic operations like NAND and NOR gates based on optical amplifier SOA. We have examine the output powers of logic levels and differentiate them . We have performed simulation at 40 Gb/s and found extinction ratio for NOR gate is 7.46dB and for NAND gate is 8.82dB. This simulation of logic gates is very useful for designing of many switching and storage devices. We have done all simulation on optical simulator OPTISYSTEM.

I. INTRODUCTION

many research scholars have been searching for optical signal processing materials for a long time that enable single light beam to be controlled by another. Although most of the optical materials are linear and allow to pass light beams through them without variation.

To achieve all optical processing functions a nonlinear optical material is used, in which different light beams can interact. In many nonlinear materials, one device has emerged as a practical solution for all-optical signal processing, the semiconductor optical amplifier (SOA).

In telecommunications applications, the benefits of the optical approach in terms of power and cost are becoming important. Telecom networks that we face today are completely based on electronic data handling, but now the data speed of a core network at 40 Gb/s (40 billion bits per second),formerly these signals were handled by CMOS silicon devices, where specialist electronic materials and sophisticated radio- frequency techniques are needed. It is difficult to track electrical signals and transmit at these speeds. The modern high-speed electronic switching equipments which are used such as an IP router .In difference this switching offers a high degree of data processing speed , the processing speed of all-optical signal is essentially high and can complex signals can be easily handled at the data rates of 40 Gb/s. SOA-based optical processing devices requires low power approximately 1W than the electronic equivalent and can be readily integrated to scale to arrays of devices that have smaller footprints. Although the individual tasks that can currently be accomplished with optical processing are relatively straightforward, these tasks such as wavelength conversion and signal regeneration are valuable in telecom networks.

By using optical networks the demand of high speed digital processing in high speed data communication, can also be increased. To perform various computational functionalities, such as packet buffering, bit-length conversions, header processing, switching, retiming and reshaping, and overcoming all the speed limitations of electronic signal processing, Photonics signal elaboration at the optical layer is attractive. A lot of attempts have been spent in these fields and one of the most capable technology to increased capacity, flexibility, and scalability to the next generation systems in the optical domain, is all-optical digital processing.

The technology all-optical signal processing is not a replacement for all electronic signal processing but by using this technology in overall optoelectronic system the effectiveness and capacity scalability can significantly increased.

Due to great potential in optical computation, several all optical Digital devices have been proposed as building elements for more complex subsystems, including optical threshold functions, logic gates, flip-flops[2], and binary counters, exploiting nonlinear effects of semiconductor optical amplifiers (SOAs). I had designed all optical AND, NAND and NOR gates.

Integrated Mach-Zahnder interferometers (MZIs)

[3] have lately been developed as very high-speed all-optical switching devices. Logic gates are the fundamental component of a fiber optic communication network. Since electronic switching is a well develop technology, it seems natural by using these switches in fiber optic networks. still the price for using this grown-up technology is optical to electrical (O/E) conversion with all the related draw backs of this method. Both O/E

and E/O conversion can be done only for a specific bit rate and data format. In addition, the high power consumption and cost associated with the amount of electronic equipment required reduce the attractiveness of this switching. The optical gate designing has been given below which can be used in optical switching as well as in optical memory.

II. DESIGN OF UNIVERSAL GATES

As we know that NAND and NOR are the universal gates means with the help of these gates we can design any combinational circuit and these gate are also very helpful in designing of sequential circuits. through this paper we have presented the design of optical circuits using NAND and NOR gate by exploring Four Wave Mixing(FWM). The block diagram of NAND and NOR gate is shown in fig. 1.

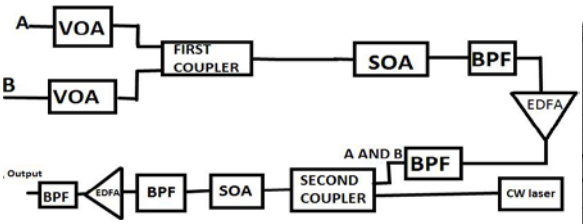


Fig 1(a) Block Diagram of optical NAND gate

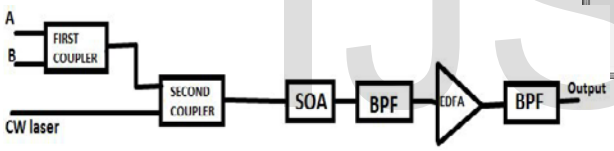


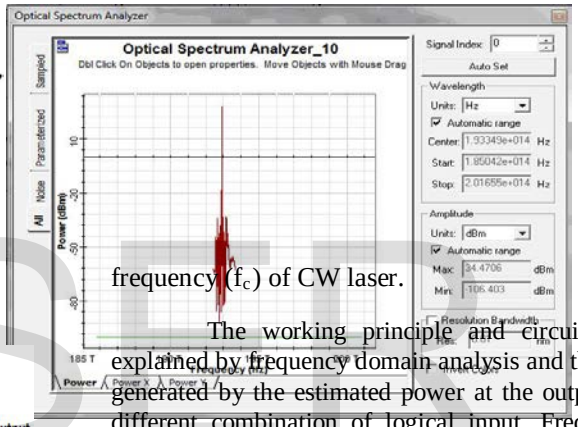
Fig 1(b) Block Diagram of optical NOR

A. Design & Simulation of optical NAND gate

The combination of a CW laser and the output of AND gate [2] is used to design the optical NAND gate as shown in fig1 (a). Two data pump generators (transmitter A and B) which carry digital data have been used to get the wanted input signal. The circuit consists of optical AND gate [2] and a probe pump (CW laser) combined at the second coupler as shown in fig 1(a). The combined output of AND gate and CW laser is given as input to the SOA, the output of AND gate is high i.e. 1, only when both the data pumps are at logic 1 if not it is low i.e. logic 0, So the FWM will generate at SOA only when both the data pumps are high "1". If any of the data pump is at logic 0, output of AND gate will be low and the output power of SOA will be equivalent to CW laser, which shows logic high level because the power of CW laser is filtered and amplified to get the NAND gate output. If both the data pumps are high then the generated FWM signal at SOA will spread the power of CW laser and a lower power level is obtained at the center frequency (f_c) of CW laser.

f_A = 193THz, f_B = 193.1THz, $f_{CW\ laser}$ = 192.9THz

As FWM will generate only when more than one signal of different frequency is given at input of SOA [4]. At the input of SOA, AND gate output and CW laser is coupled. When one or both the data pumps are at logic low i.e. 0 FWM will be generated because output of AND gate will be 0 and the output will be corresponding to the peak of CW laser, as shown in fig 2.



The working principle and circuit functioning is explained by frequency domain analysis and the logic output is generated by the estimated power at the output equivalent to different combination of logical input. Frequencies of data pumps and probe pumps are taken as below.

Fig 2: Sectrum analyzer at the output of second SOA when both inputs are low

Output of AND gate is high only when both the inputs are high so the output of AND gate and CW laser will together generate the FWM signal as shown in fig 3.

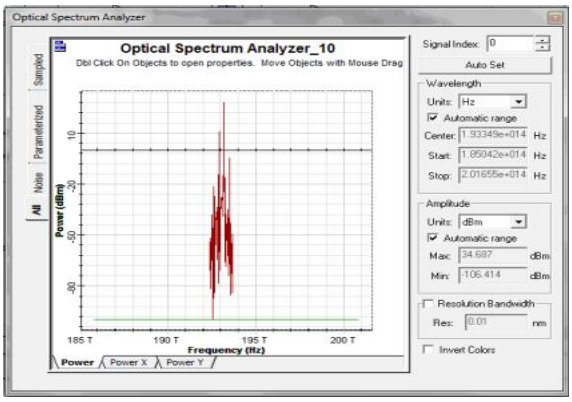


Fig 3: Spectrum analyzer at the output of second SOA when both inputs are high

Output of SOA is filtered about the centre frequency of the BPF of CW laser. Now This filtered output is amplified by linear amplifier i.e. EDFA and is again filtered through the BPF to remove the unnecessary signal(noise). So a lower value of output power will be obtained when FWM will be generated and output will be considered as logic 0. For output power calculation time domain visualizer and power meter used for different input sequences as shown in fig 4-7.

1. A=0 and B=0

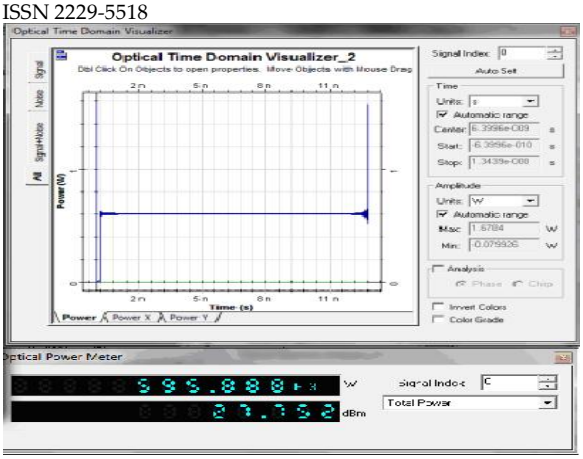


Fig 4: Time domain visualizer and optical power meter output at A=0, B=0

2. A= 0 and B=1

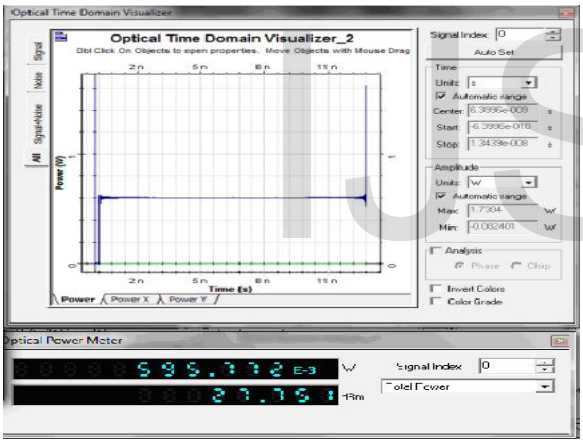


Fig 5: Time domain visualizer and optical power meter output at A=0, B=1

3. A=1 and B=0

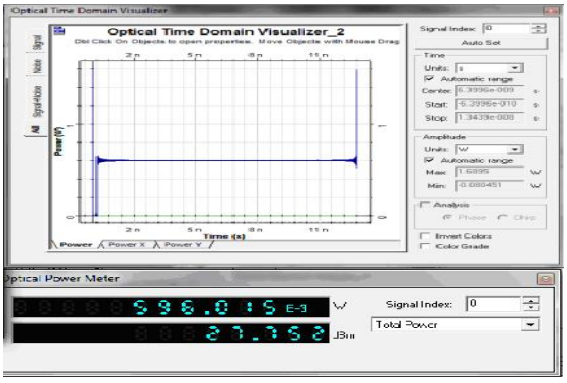


Fig 6: Time domain visualizer and optical power meter output at A=1, B=0

4. A=1 and B=1

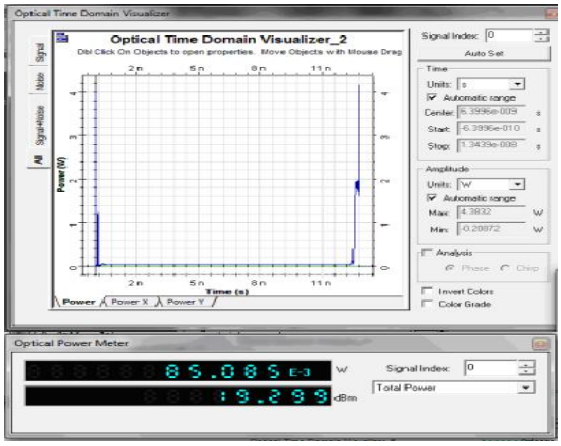


Fig 7: Time domain visualizer and optical power meter output at A=1 and B=1

Truth table obtained from the time domain analysis and power meter outputs corresponding to input signals are as below.

1. TABLE I: Truth table of Optical NAND gate

S.No.	A	B	Output Power(W)	Output power (dB)	Logic
1	0	0	595.888e-3	27.752	1
2	0	1	595.772e-3	27.751	1
3	1	0	596.015e-3	27.752	1
4	1	1	85.085e-3	19.299	0

From above truth table it is clear that the output is high when any of the input bits is low. So we can conclude that it is a truth table of NAND gate.

B. Design and simulation of Optical NOR gate

In the design of Optical NOR gate two data pumps (A and B) which can carry data signals and a probe pump (CW Laser) is used to generate the logic of NOR gate. The output of two data pumps are coupled together by the first coupler to get a logic of OR gate i.e the output will be high when any one of the input is high, this output is coupled with probe pump by second coupler and the output of this second coupler is fed to the SOA. Now three signals of different frequency is given as input to the SOA, these input signals will generate the FWM signal when any two inputs signal are high. When any of transmitter (data pump) is at logic „1" it will generate the FWM signal with probe pump (CW laser). The power of each data pump and probe pump is coupled together, When FWM signal is generated it spreads the power of CW laser and if we filter the signal of CW laser by BPF (tuned at the frequency of probe pump), a lower value of power will be obtained which can

be considered a logic „0". When both the data pumps are at logic „0" no FWM signal will be there at the output of SOA, so the total power of CW laser will be there at the output of BPF and it can be considered as logic

„1". The signal of CW laser is selected by first BPF and amplified; this amplified signal is again passed through the second BPF with the center frequency of CW laser to remove the unwanted signals.

The frequencies of data pumps and probe pump are taken as below.

f_A = 193THz, f_B = 193.1THz, $f_{CW\ laser}$ = 192.9

When both the inputs are high i.e logical input given to the transmitter A and B is logic "1", FWM is generated at output of SOA as shown in figure 8. FWM is showing the spread of total power at different peaks.

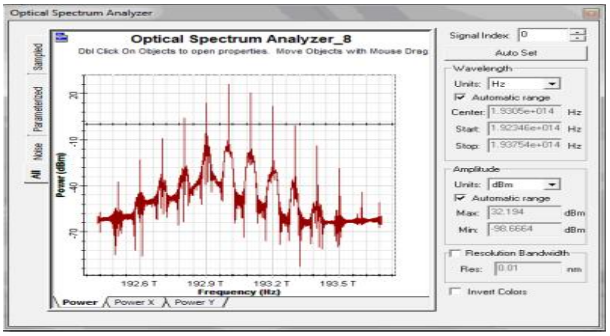


Fig 8: Spectrum analyzer at output of SOA (FWM Generation) when both inputs are high

As the BPF is set at the frequency of CW laser i.e. at 192.1THz, it will pass only one peak equivalent to CW laser which is less than the threshold level because total power of CW laser is used to generate number of peaks as shown in fig.10 and is detected as 0. If only one data pump is high, it again generates the FWM signal with CW laser and a lower value of output power will be obtained.

When the input bit at the bit sequence generator of both the transmitter is 0 then there will be no optical signal received at the output of first coupler and at the second coupler only the optical power corresponding to CW laser will be obtained. Then the output of second coupler is given as input to the SOA. Therefore the peak corresponding to the CW laser is obtained, which is then filtered by BPF with the center frequency of 192.1THz and amplified. This amplified signal is again filtered to remove the unwanted signals. Since the total power of CW laser is taken at output, it will generate logic1 at the output, as

shown in fig 9.

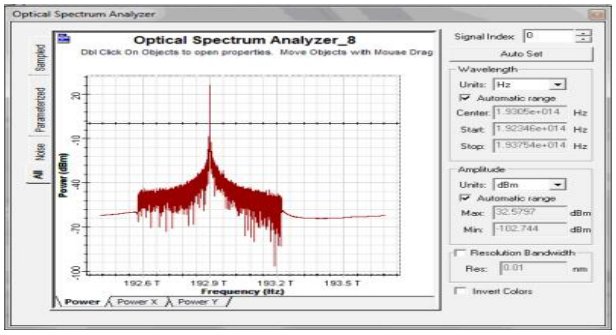


Fig 9: Spectrum analysis at the output of SOA when both inputs are zero

For output power calculation time domain visualizer and power meter is used for different combination of input sequences as shown in figure 10-13.

1. A=0 and B=0

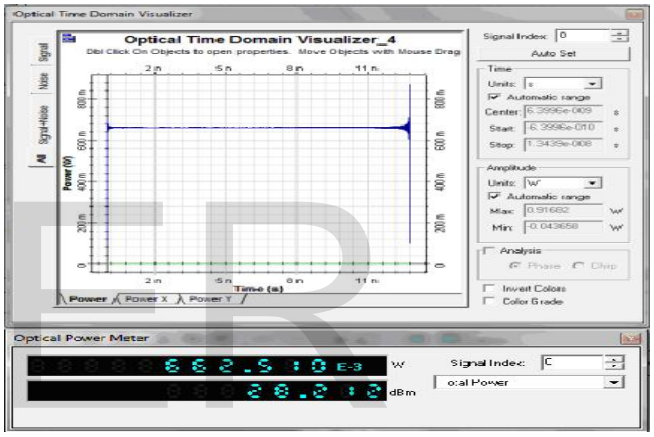


Fig 10: Output of time domain visualizer and power meter at A=0 and B=0

2. A=0 and B=1

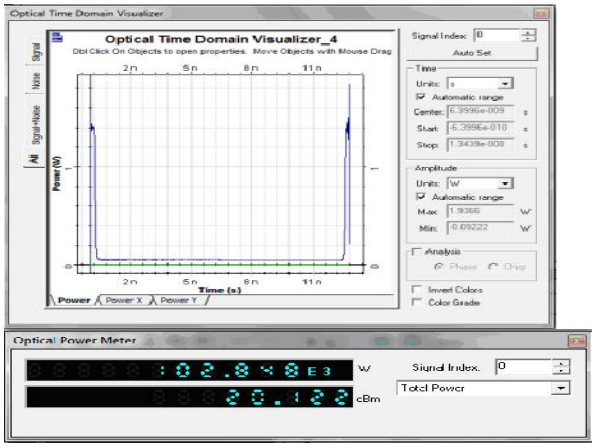


Fig 11: Output of time domain visualizer and power meter at A=0, B=1

3. A=1 and B=0

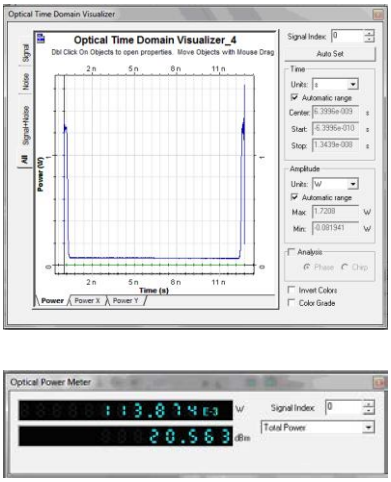


Fig 12: Output of time domain visualizer and power meter at A=1, B=0

4. A=1 and B=1

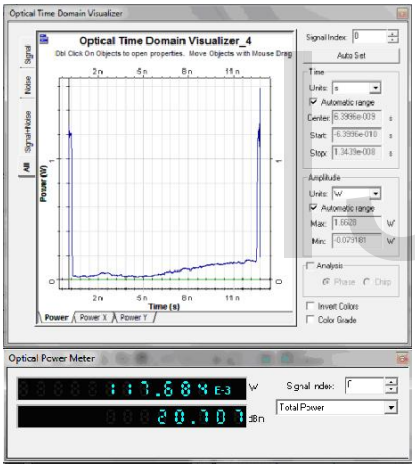


Fig 13: Output of time domain visualizer and power meter at

Above results are corresponding to different logical inputs, so to generate the logic at the output, truth table is prepared as follows

2. TABLE II: Truth table for optical NOR gate

S.No.	A	B	Output Power(W)	Output power (dB)	Logic
1	0	0	662.510e-3	28.212	1
2	0	1	102.848e-3	20.122	0
3	1	0	113.874e-3	20.563	0
4	1	1	117.684e-3	20.707	0

From above truth table we can see that the output power is low when any of the input bit is high, so we conclude that the output power is corresponding to a logic of NOR gate.

III. Conclusion

In this paper , we have numerically simulated all-optical logic gates NOR and NAND gates at 40 Gb/s in optical switching network. The analysis of the extinction ratio and output power for the two logic levels(Low and high) various signal parameters such as input optical power, SOA active length region and SOA current gain has been varied with respect to time. These gates can be used for designing many switching and storage devices like all universal gates. Hence these optical gates can be the key elements in next-generation optical networks in LAN and WAN environment with advance multiplexing like WDM. These gates has a great role computing systems to perform optical signal processing functions such as all-optical label swapping[5], wavelength converter, header recognition[6][7], parity checking, binary addition, and data encryption. The outputs of time domain visulizer are determining the power levels of logic gates with on condition and off condition like logic low and logic high. Table I and II concludes the truth tables of NAND and NOR gates.

REFERENCE

[1]J. H. Lee, T. Nagashima, T. Hasegawa, S. Ohara, N. Sugimoto, and K.

Kikuchi, “40 Gbit/s XOR and AND gates using polarization switching within 1 m-long bismuth oxide-based nonlinear fiber,” Electron. Lett., vol. 41, no. 19, pp. 1074–1075, 2005.

[2]Jing Wang, Gianluca Meloni, Gianluca Berrettini, Luca Pot`ı, and Antonella Bogoni”all optical Clocked flip flops and binary counting operation using SOA – Based SR latch and logic gate”, 1077-260X © 2010 IEEE

[3]Martin T. Hill, H. de Waardt, H.J.S. Dorren,”fast all optical flip flop using coupled Mach-Zehnder Interferometer” Department of Electrical Engineering, EH 12.33, Eindhoven University of Technology, PO. Box 513, 5600 MB Eindhoven, The Netherlands.E.Mail: m.t.hill@ele.tue.nl.

[4]Osamu Aso, Masateru Tadakuma and Shu Namiki “Four-Wave Mixing in Optical Fibers and Its Applications”, WP Team, Opto-technology Lab., R & D Div, www.scribd.com.

[5]J. M. Martinez, J. Herrera, F. Ramos, and J. Marti, “All-optical address recognition scheme for label-swapping networks,” IEEE Photon. Technol. Lett., vol. 18, no. 1, pp. 151–153, Jan. 1, 2006.

[6]J. M. Martinez, F. Ramos, and J. Marti, “All-optical packet header processor based on cascaded SOA-MZIs,” Electron. Lett., vol. 40, no. 14, pp. 894–895, 2005.

[7]S. A. Hamilton and B. S. Robinson, “40-Gb/s all-optical packet synchronization and address comparison for OTDM networks,” IEEE Photon. Technol. Lett., vol. 14, no. 2, pp. 209–211, Feb. 2002.